

**REMARKS**

The allowance of claim 9 is gratefully acknowledged by the Applicant.

Claims 1, 9 and 10 have been amended. New claim 11 has been added. The application contains pending claims 1 and 9-11, of which claim 9 has been allowed. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications.

The specification has been amended to fill in the patent number of the parent application. No new matter has been added.

Applicant filed an Information Disclosure Statement (IDS) on January 16, 2004. The Office Action did not acknowledge the IDS. Applicant respectfully requests that the Examiner consider and acknowledge the references submitted in the IDS. For the Examiner's convenience, Applicant has attached a copy of the IDS citation sheet submitted with the January 16, 2004 IDS. Applicant respectfully requests that the Examiner initial and return the IDS citation once the references have been considered.

Claims 1 and 10 stand rejected under 35 U.S.C. § 102(b) as being anticipated by JP 11-162003. The rejection is respectfully traversed.

Claim 1 recites an optical pickup device comprising a light source, a plurality of light receiving members and a signal processing circuit. According to claim 1, the signal processing circuit converts "current signals output from each of the plurality of light receiving members into voltage signals, add[s] the voltage signals to obtain an added voltage signal, and attenuate[s] a level of the added voltage signal." Applicant respectfully submits that JP 11-162003 fails to disclose the claimed invention.

The Office Action states that JP 11-162003 teaches the use of a signal processing unit for converting the signal from the photo detectors into voltages (I/V converters Fig. 7) and processing circuit 5 having elements 501, 502 and 504 in order to attenuate the summed signal from the added (RF signal) from the photo detection means. The Office Action indicates that "attenuate" reads on any element that alters the added signal. Applicant respectfully traverses these arguments.

Applicants respectfully submit that circuit element "5" in JP 11-162003 is a "data reproducing section." The data reproducing section 5 includes an equalizer 501, a binarization circuit 502, a demodulating and ECC circuit 503, and a PLL 504. The equalizer 501 emphasizes a predetermined frequency component. There is nothing in the data reproducing section 5, or any component of JP 11-162003, that "attenuates" a summed signal from light receiving elements. Attenuation is not merely "altering" as suggested by the Office Action. An equalizer, such as the one disclosed in JP 11-162003, does not attenuate. As such, JP 11-162003 fails to disclose a signal processing circuit to "attenuate a level of the added voltage signal" as recited in claim 1. Therefore, Applicant respectfully submits that claim 1 is allowable over JP 11-162003.

Claim 10 also recites "means for converting current signals output from each of the plurality of light receiving members into voltage signals, adding the voltage signals to obtain an added voltage signal, and attenuating a level of the added voltage signal." As such, claim 10 is allowable over the cited reference for at least the reasons set forth above and on its own merits. Accordingly, it is believed that claims 1 and 10 are allowable over JP 11-162003. The rejection should be withdrawn and the claims allowed.

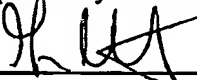
Claims 1, 9 and 10 have been amended solely to clarify the claims and not for purposes of patentability.

New claim 11 has been added and is believed to be allowable for at least the reasons set forth above and on its own merits.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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